



Understanding and performing MIPI M-PHY Physical and Protocol Layer Testing

Transmitter, Receiver and UniPro/LLI/DigRFv4

Application Note

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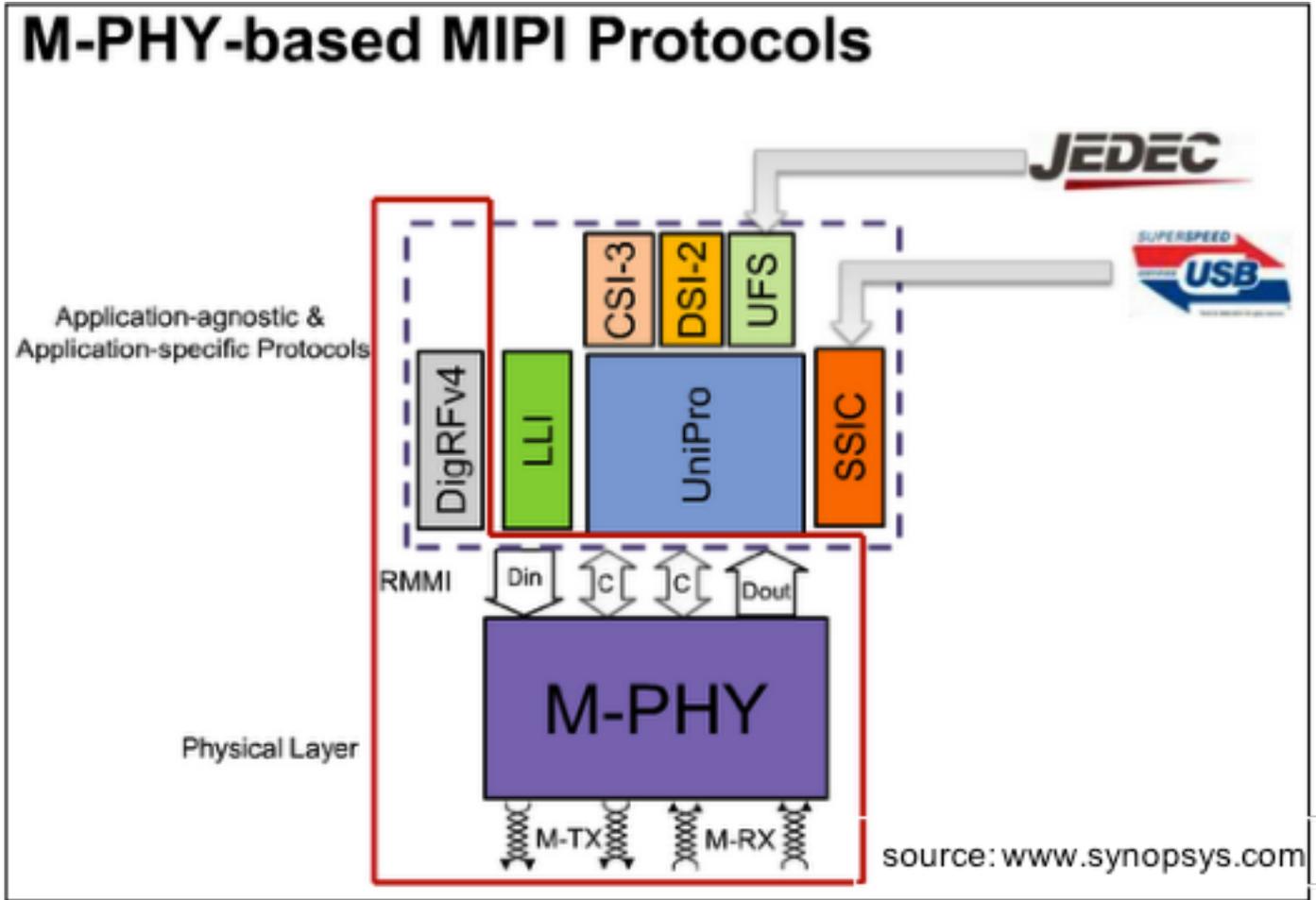


Figure 1-1.

1 Introduction

M-PHY is a high-speed serial physical interface to the DigRFv4, UniPro, LLI, CSI-3 and DSI-2 protocol interconnect standards of the MIPI Alliance, and the UFS and SSIC protocol standards of JEDEC and USB-IF respectively.

With Flexible signal characteristics, M-PHY will be used in the development of mobile devices that offer increased performance, effective power management schemes, robustness against RF interferences and low RF emission. It is expected to see broad adoption across the mobile device and portable PC (tablet) industry in the next few years.

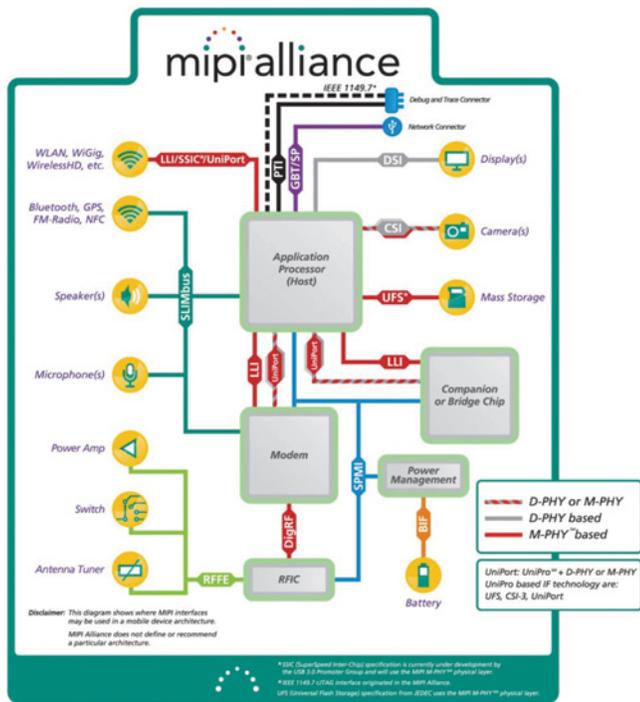


Figure 1-2. Source: MIPI Alliance, www.mipi.org

2 Technology Background

MIPI provides specifications for standard hardware and software interfaces within a mobile device. MIPI specifications improve interoperability between components from different component vendors, reduces the effort of integration and speed up the time-to-market for mobile terminals.

One of the primary roles of MIPI standards is to convert legacy parallel interfaces into modern serial data interfaces. As a result, all MIPI standards are serial data and follow a set of protocol stacks. Figure 1-2 shows an overview of application areas in a mobile design against the applicable MIPI protocol layer standards.

The physical layer standards include D-PHY, M-PHY, SlimBus, HSI, and DigRF 3G. The two PHY layers, D-PHY and M-PHY, are expected to coexist for a long time. Both are reusable, scalable physical layers for the various components on a mobile terminal.

First out of the chute, D-PHY differs significantly from many existing mobile interfaces because it can switch between the differential high-speed (HS) and the single-ended low-power (LP) modes in real time depending on the need to transfer large amounts of data or to conserve power to prolong the battery life. The D-PHY interface is capable of operating in simplex or duplex configurations with a single data lane or multiple data lanes. The clock is always master to slave and in quadrature phase with data.

Even though D-PHY is a capable interface, since it is synchronous, speed is limited to 1.5 Gbps, preventing it from supporting applications that require higher data transfer rates. That's where M-PHY, approved in late 2010, comes in. It is a much more powerful PHY designed to handle the ever-increasing data bandwidth requirement of mobile devices.

M-PHY offers asynchronous data rates exceeding 5 Gbps, giving designers the ability to speed up memory transfer and CSI/DSI interface speeds. In addition to higher speeds, the M-PHY will use fewer signal wires because the clock signal is embedded with the data through the use of 8b/10b encoding. M-PHY is optical friendly. M-PHY is used as physical layer for DigRF v4, LLI, SSIC and UniPro.

DigRF v4 is used in mobile terminals that support next generation mobile broadband technologies such as Long Term Evolution (LTE) and mobile WiMax. DigRF is an interface standard between one or more Baseband ICs(BBICs) and Radio Frequency ICs(RFICs) in a single terminal. Main purpose of DigRF specification is to increase bandwidth capability to support data rates of LTE, WiMax etc, minimize interface pin count, minimize interface power consumption, manage EMI issues and interoperability with different transceivers.

LLI is a low latency, bidirectional point to point interface which enables two chips to communicate efficiently.

The Low Latency Interface (LLI) is a point-to-point interconnect that allows two devices on separate chips to communicate as if a device attached to the remote chip is resident on the local chip.

SSIC (Super Speed Inter-Chip) is an optimized inter-chip version of USB3.0. SSIC uses the MIPI M-PHY specification as the physical layer of the interconnect to meet the requirements of embedded inter-chip links.

UniPro(Unified Protocol) defines an application-agnostic scalable layered protocol for interconnecting devices and components within a mobile terminal. UniPro allows these devices and components to exchange data at high data rates, with low pin count and at low energy per transferred bit. The networking capabilities of UniPro enable the emergence of sub-systems such as (but not limited to): memory sub-systems, connectivity sub-systems or imaging sub-systems.

M-PHY is a successor of D-PHY, requiring fewer pins and providing more bandwidth per pin with improved power efficiency. In M-PHY data transfer occurs in burst or in continuous mode and it can be in high speed(HS) or low speed(LS).

M-PHY supports two drive strengths, Large Amplitude(LA) and Small Amplitude(SA). M-PHY supports two types of modules – Type-I and Type-II based on signaling scheme used in low speed mode. Low speed mode can use either Pulse Width Modulation (PWM) or Non Return to Zero (NRZ) as signaling scheme.

DigRFv4 supports Type-II module, SSIC, LLI and UniPro supports Type-I module.

M-PHY Signal Characteristics									
Signaling mode	Datarates			Amplitudes		Impedance			
	Gears	A (Gbps)	B (Gbps)	Large	Small	Resistive Terminated	Non Terminated		
High Speed (HS)	G1	1.248	1.4576	Terminated: 160-240mV, Non-Terminated: 320-480mV	Terminated: 100-130mV, Non-Terminated: 200-260mV	50 ohms	-		
	G2	2.496	2.9152						
	G3	4.992	5.8304						
PWM (ie. TYPE-I)	Gears	Min (Mb/s)	Max (Mb/s)					50 ohms	10k ohms
	G0	0.01	3						
	G1	3	9						
	G2	6	18						
	G3	12	36						
	G4	24	72						
	G5	48	144						
	G6	96	288						
G7	192	576							
SYS (i.e TYPE-II)	-	-	576 (Mb/s)			50 ohms	10k ohms		

Table 3-1.

3 Transmitter Testing

3.1 Transmitter Configurations and Testing Challenges

3.2 High Speed measurements

This group of tests verifies various transmitter signaling and timing requirements of an M-PHY transceivers, defined in M-PHY specification. High speed mode is common for both Type-1 and Type-2 modules and hence all tests related to HS mode are required for all modules. There are various performance parameters which need to be measured on HS mode signals like – slew rate, transition time, pulse width, unit interval, differential DC and common mode voltage, minimum eye opening, Power Spectral Density(PSD), jitter(long term and short term).

Except PSD, all other parameters are either related to time or voltage and can be easily measured using an oscilloscope.

Performing PSD measurement on an oscilloscope is a challenge and it is addressed in section 3.2.3.

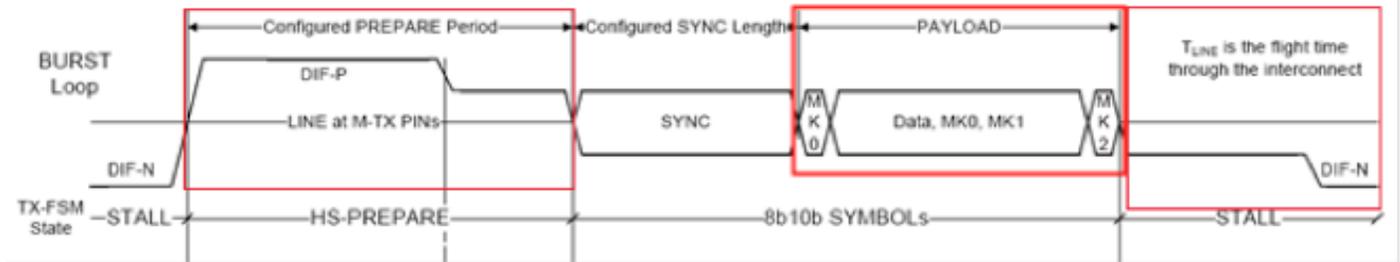


Figure 3.1. M-Phy Burst states (Source - M-PHY Physical Layer Conformance Test Suite v0.8).

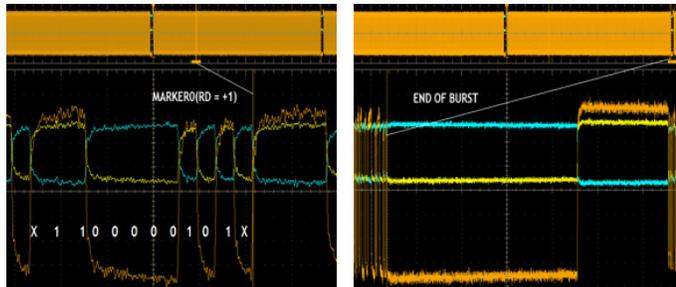


Figure 3.2.

3.2.1 Test Signal Validation

In MPHY high speed measurements, signal validation is done for each acquisition. As part of signal validation, following parameters are validated/checked on the acquired signal

- **Data Rate**
Unit interval of an MPHY burst data signal need to be computed. Data rate variations could be within 2000ppm for any HS gear.
- **MARKER0**
MARKER0 (considering both positive and negative disparity) is searched in the acquired waveform. If MARKER0 is present, then the signal validation is passed for this parameter.

3.2.2 Cursor Gated Measurements

In MPHY, data transmission can happen in burst or continuous mode. In burst mode data transmission, a burst will have different states like – PREPARE, SYNC, MK0, PAYLOAD, STALL. MPHY has certain electrical parameters which need to be measured at specific states of the burst. For example – PREPARE length uses PREPARE state, differential DC positive and negative use PREPARE and STALL respectively, EYE, jitter, transition time and unit interval use MK0, PAYLOAD and MK2 only. So as a pre-requisite, one has to identify different states in a burst waveform, place markers/cursors and then measure the required electrical parameter.

MPHY burst has SYNC and PAYLOAD which are 8b10b encoded and hence there are no symbols which have more than five continuous ones or zeros(maximum allowed run length of 5 bits). This property is used to identify PREPARE and STALL. Remaining part of the waveform(SYNC, MK0, PAYLOAD and MK2) are converted into bits, location of MK0(considering both positive and negative disparity), end of burst are identified and measurements are performed on cursor gated regions.

3.2.3 PSD measurement

M-PHY is used as a physical layer in DigRF for communicating between baseband and radio frequency ICs. Bit rates of M-PHY are high enough to be in and around the operating bands of the radios in mobile systems. Electromagnetic interference (EMI) radiating from the serial interface will interfere with the mobile device's radio low noise amplifier. It is found that the common-mode signal component dominates EMI interference. As part of M-PHY transmitter compliance testing, one has to make sure that PSD of common mode signal is within the mask defined by below mathematical expression.

$$CMMask(f_{MHz}) = -180 - (14.3 * \log(f_{MHz}) - 159) \frac{dBm}{Hz} \quad 500 < f_{MHz} < 4000$$

Usually PSD is computed using a spectrum analyzer and this results in usage of both oscilloscope and spectrum analyzer for M-PHY transmitter tests. But Tektronix provides a single box solution for all M-PHY transmitter tests. Computing Power Spectral Density using an oscilloscope is a challenge and it is overcome as follows:

- TxDp and TxDn signals are given as inputs to oscilloscope
- Common mode signal is computed using oscilloscope math function.
- Common mode signal is passed through hamming window.
- FFT of windowed common mode signal is computed using an in built scope FFT module.
- An average of spectral magnitude of N acquisitions is computed. Let this average result be "X".
- PSD in dBm/Hz is computed using the following mathematical equation

$$PSD = 20 * \log_{10}(X) - 10 * \log_{10}(R) - 10 * \log_{10}(RBW) + 10 * \log_{10}(1000)$$

where

R = 25 Ohm, the common mode resistance

RBW = Resolution Band Width = 1.3/ (Gating Duration)

[Factor of 1.3 is due to Hamming Window]

Factor of 1000 is to convert dB to dBm

- Minimum PSD margin is computed as,
PSDMargin = Minimum(CMmask – PSD)
- If minimum PSD margin is greater than zero, then PSD of common mode signal is considered to be within EMI limits.

3.3 PWM Measurements

The M-PHY Conformance Test Spec v0.8 lists the following ten measurements for PWW TX

1. Transmit Bit Duration
2. Transmit Ratio
3. TX Prepare Length
4. Common Mode DC
5. Differential DC
6. Differential AC
7. Rise/Fall Time
8. Lane to Lane Skew
9. Bit Duration Tolerance
10. Minor Duration

Scopes Support for MPHY HS TX								
		DPO/DSA/MSO	DPO/DSA/MSO	DPO/DSA/MSO	DPO/DSA/MSO	DPO/DSA/MSO	DPO/DSA	DPO/DSA
		70604, B and C	70804, B and C	71254, B and C	71604, B and C	72004, B and C	72504D	73304D
		BW=6 GHz, RT=45 pS	BW=8 GHz, RT=34 pS	BW=12.5 GHz, RT=22 pS	BW=16 GHz, RT=17 pS	BW=20 GHz, RT=14 pS	BW=25 GHz, RT=12 pS	BW=33 GHz, RT=9 pS
G1A	DR=1248 Mbps, RT=80.128 pS	Yes	Yes	Yes	Yes	Yes	Yes	Yes
G1B	DR=1457.6 Mbps, RT=68.606 pS	Yes	Yes	Yes	Yes	Yes	Yes	Yes
G2A	DR=2496 Mbps, RT=40.064 pS	No	Yes	Yes	Yes	Yes	Yes	Yes
G2B	DR=2915.2 Mbps, RT=34.303 pS	No	Yes	Yes	Yes	Yes	Yes	Yes
G3A	DR=4992 Mbps, RT=20.032 pS	No	No	No	No	Yes	Yes	Yes
G3B	DR=5830.4 Mbps, RT=17.151 pS	No	No	No	No	Yes	Yes	Yes

Table 3-2.

3.4 Choice of Oscilloscope and Probes

MPHY has two modes of operation – High speed and Low power. In high speed mode, the data rate ranges from 1248 Mbps to 5830.4 Mbps. In low power mode, the data rate ranges from 10 kbps to 576 Mbps. While choosing test equipment (oscilloscope and probes), one has to make sure that

- the bandwidth of the test system(combined bandwidth of oscilloscope and probe) allows at least the fifth harmonic of the highest frequency(half of the data rate for NRZ signal) present in the signal
- transition time of the test system(combined transition time of oscilloscope and probe) is smaller(faster transition) than the signal transition time

Considering bandwidth and transition time, choice of the oscilloscope for different gears (HS and PWM) is as given in Table 3-2. All PWM gears are supported by all the oscilloscopes listed in Table 3-2 .

Probes Support for MPHY HS TX									
		P7360A	P7380A	P7313	P7506	P7508	P7513A	P7516	P7520
		BW=6 GHz, RT=52.5 pS	BW=8 GHz, RT=41.25 pS	BW=13 GHz, RT=30 pS	BW=6 GHz, RT=56.25 pS	BW=8 GHz, RT=41.25 pS	BW=13 GHz, RT=30 pS	BW=16 GHz, RT=24 pS	BW=20 GHz, RT=21.75 pS
G1A	DR=1248 Mbps, RT=80.128 pS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
G1B	DR=1457.6 Mbps, RT=68.606 pS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
G2A	DR=2496 Mbps, RT=40.064 pS	No	No	Yes	No	No	Yes	Yes	Yes
G2B	DR=2915.2 Mbps, RT=34.303 pS	No	No	Yes	No	No	Yes	Yes	Yes
G3A	DR=4992 Mbps, RT=20.032 pS	No	No	No	No	No	No	No	Yes
G3B	DR=5830.4 Mbps, RT=17.151 pS	No	No	No	No	No	No	No	Yes

Table 3-4.

Additionally, the maximum input voltage is also considered while choosing probes. Choice of probes for different gears (HS and PWM) is as given in Table 3-4. All SMA Probes with bandwidth greater than 6GHz are suitable for PWM mode.

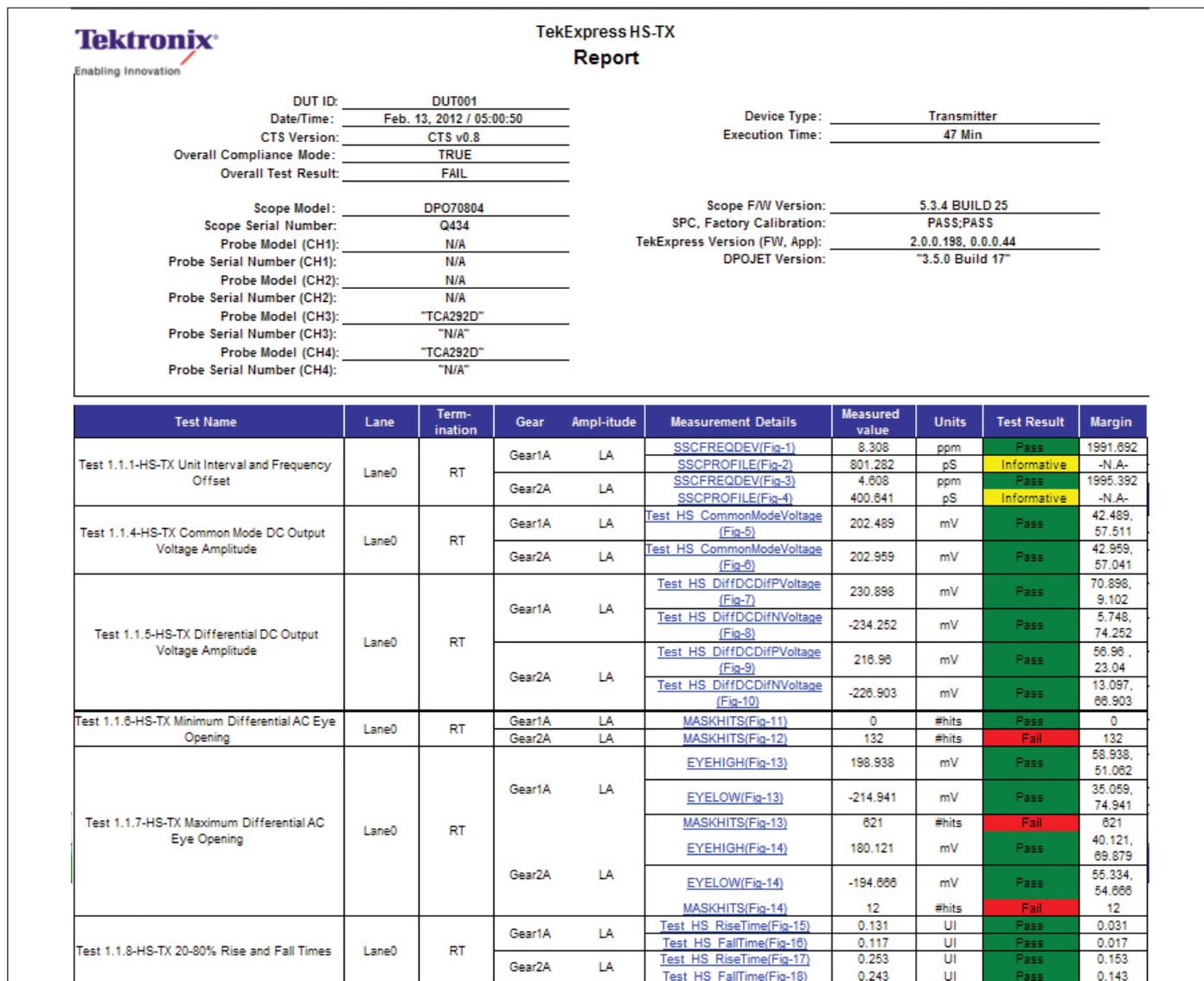


Figure 4-1.

4 Transmitter Test Solutions

4.1 Automated M-PHYTX

The M-PHYTX automated software from Tektronix provides following features and benefits for M-PHY transmitter testing.

- Automated testing reduces the complexity of executing transmitter tests and enables you to test devices faster
- Highly optimized setup performs Power Spectral Sensity (PSD) tests using oscilloscope-integrated algorithms uniquely, and does not require an external spectral analyzer or extra hardware to perform PSD measurements
- Automates the most complete 95% test coverage of high speed, and 75% test coverage of PWM measurements
- Seamless debug allows pause on each test in automation, and switch to dpojet analysis tool for detailed debug
- Configuration for regression allows selecting different gears and sub-gears of HS and PWM signals, large/small amplitudes, impedance termination/un-termination
- Single printable report for approximately 1000 tests across different combinations, provides pass/fail summary table, along with margin details, optional waveform captures, and eye diagrams.

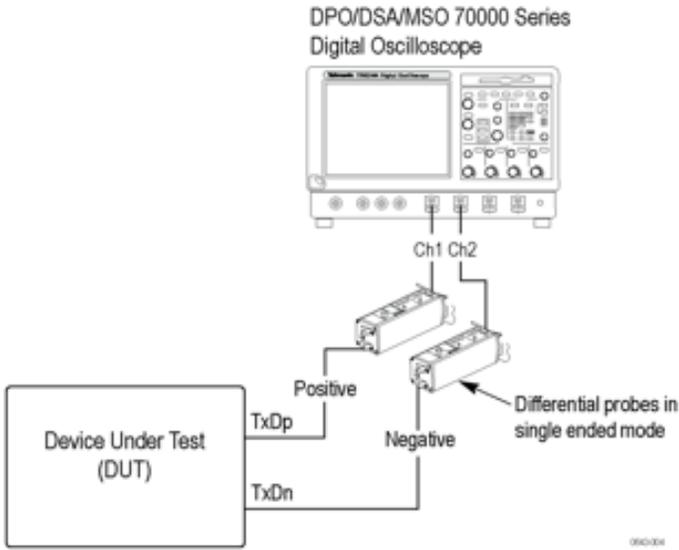


Figure 4-2.

4.1.1 Simple Test Setup

Test setup and test execution is very simple with the M-PHYTX Automation software. The test setup connections are very minimal, as it involves only one piece of equipment for M-PHYTX. The TekExpress software provides a Graphical User Interface (GUI) and an intuitive workflow through setup and testing.

4.1.2 Multi-lane Testing with M-PHYTX

M-PHYTX software in differential mode of acquisition enables multi-lane M-PHY setups. This means that four lanes of an M-PHY transmitter can be connected simultaneously to four channels on an oscilloscope providing faster test set-up and shorter run times.

4.2 Customizable Setup Libraries using opt.M-PHY DPOJET

DPOJET software with Option M-PHY provides the essential set of M-PHY Transmitter measurement setup libraries with greater flexibility in the test setup. Like the D-PHY Essentials on DPOJET, the M-PHY Essentials software also enables Characterization, Debug, Analysis, and Conformance testing of M-PHY designs.

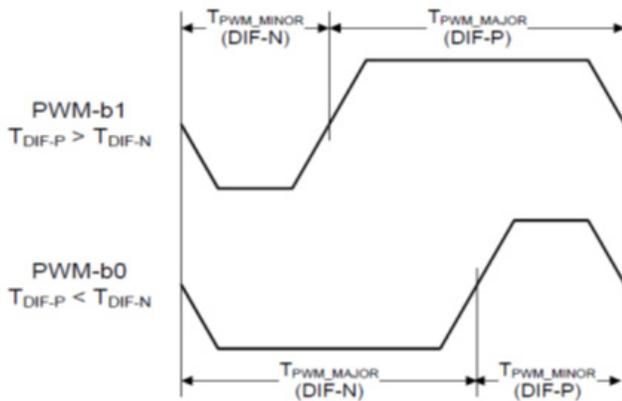


Figure 5-1. PWM-bit1 and PWM-Bit0^[Ref 1].

5 Receiver Testing

5.1 Different Signal Generation requirements

Receiver testing has many waveform generation needs such as NRZ(Non-return to Zero) signaling and PWM(Pulse Width Modulation) signaling, 8b/10b encoding, Reference clock, Differential signal generation with common mode DC, and addition of jitter impairments like – ISI, Pj, Rj.

5.1.1 PWM Signaling

PWM or Pulse Width Modulation signaling has self-clocking properties. PWM is used in the Low speed mode of MPHY, for mostly control commands

Each bit consists of a combination of two sub-phases, a DIF-N followed by a DIF-P. One of the two sub-phases is longer than the other $TPWM_MAJOR > TPWM_MINOR$, depending upon whether a binary one, or binary zero is being sent^[1]. In this case the bit duration is defined as $TPWM_TX = TPWM_MINOR + TPWM_MAJOR$. Figure 5-1 shows the PWM-bit0 and PWM-bit1 showing the minor and major regions.

Figure 5-1 shows PWM-Bit1 and PWNBit0 NRZ waveform and PWM waveform for the bit stream: 110110, respectively.

PWM is employed as Low Speed Mode of MPHY.

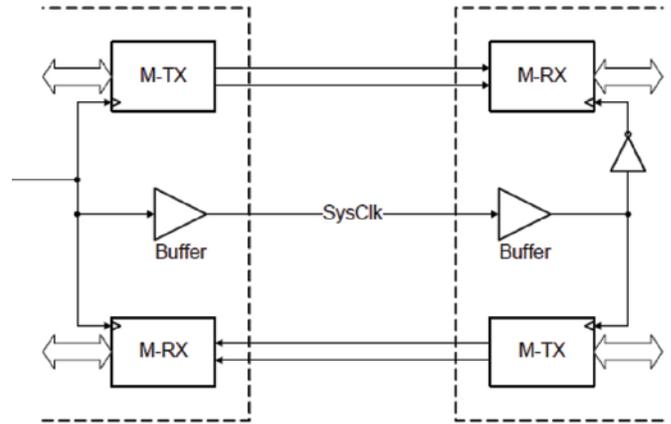


Figure 5-2. Bidirectional SYS-Burst clocking example (Image taken from Specification).

Reference Frequency(MHz)	Interface data rate
26 / 38.4 / 52	26 / 38.4 / 52

Table 5-1. Bidirectional SYS-Burst clocking example (Image taken from DigRFv4 Specification).

5.1.2 SYS Mode(System-clock Synchronous Mode)

SYS mode is a low speed transmission mode supported by type-II modules. Data is 8b10b encoded and transmitted using reference clock synchronous NRZ signaling. SYS mode requires clock for sampling the data. The transmission rate in this mode shall be an integer division of the shared reference clock frequency, f_{SYS_REF} . The reference clock may originate from an independent system clock or from one of the two devices in the LINK.

DigRFv4 uses SYS mode for low speed transmission. In DigRFv4, supported low speed data rates are given in Table 5-1.

In low speed mode, there is no synchronization pattern upon exiting SLEEP state. The data is transferred synchronously in both directions across the interface and therefore there is no need for the clock data recovery algorithm and synchronization pattern.

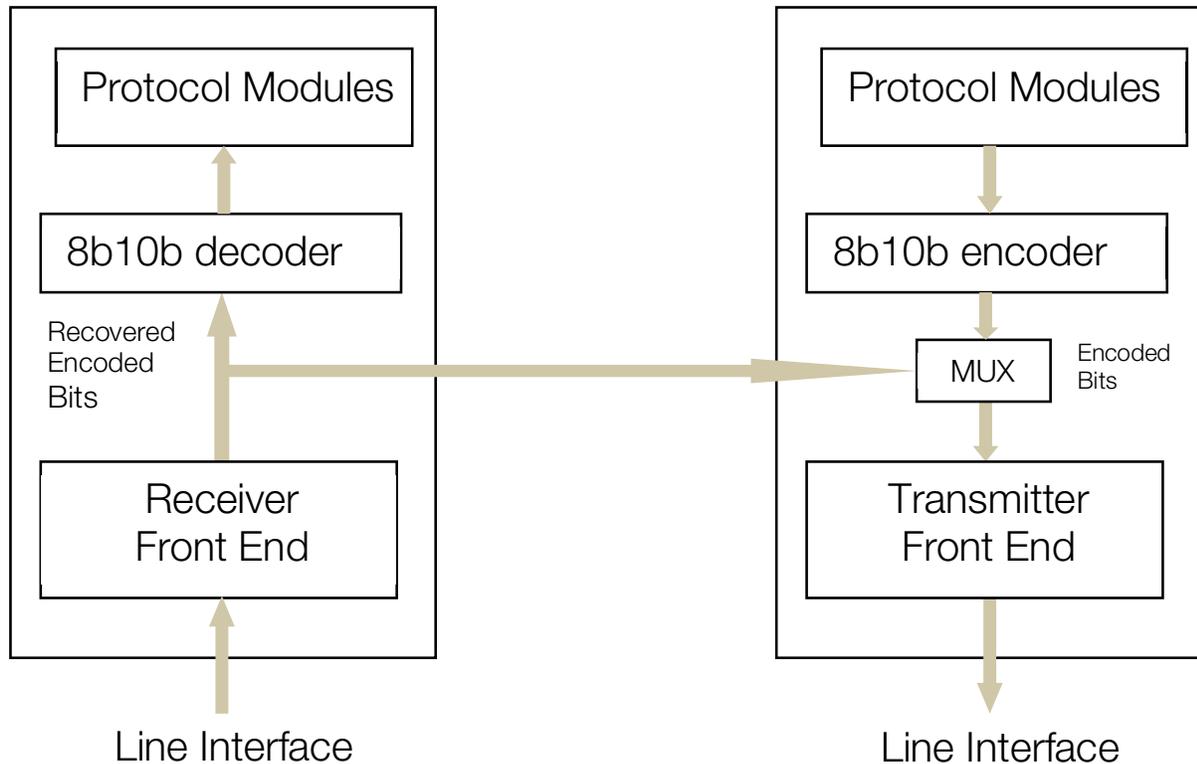


Figure 5-3. Device loopback mode for receiver validation.

5.2 Design Validation

5.2.1 Receiver Loopback Mode

Loopback mode is one of the most common mechanisms used for receiver testing. In this mode, data that is received at the RX is retransmitted out of the TX.

In M-PHY loopback, the receiver routes/re-transmits the recovered M-PHY signal via the transmitter. Receiver will not do decoding of 8b10b symbols. Loopback mode requires both transmitter and receiver to be configured to same MODE and GEAR. Loopback mode is used for BER testing. And, an Oscilloscope based Error Detector will enable performing the above BER testing.

5.2.2 Receiver Non-Loopback Mode

For Non-loopback mode setups, the DUT must be placed into a mode where simple, framed patterns containing valid CRC's can be sent into the receiver, using a non-protocol-aware signal generator (example an AWG7000). Most current lab signal sources contain some degree of sequencing capability that can be used to send startup/configuration information prior to a repeating test sequence.

If a mode exists where a receiver is able to verify CRC-checked frame data, a mechanism must be provided that allows for observation of the results of the checking operation. While this may be achieved through internal vendor-specific registers and counters, it is also possible (and preferable) to allow this to be performed through the Physical Layer interface.

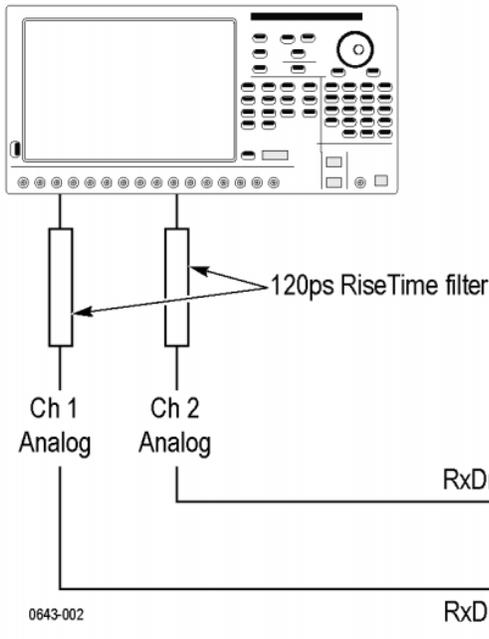
5.2.3 Receiver Jitter Tolerance

M-PHY Rx specifies Long term Jitter (TJ) and Short Term Jitter (STJ), to specify the receivers jitter tolerance [new cocktail of the jitter budget expected in the next spec version].

SHORT TERM JITTER: This includes ISI of 0.2UI and Random jitter of 0.1UI.

LONG TERM JITTER : Total jitter of 0.52UI includes Periodic jitter(PJ) of 0.22UI, in addition to the STJ components. PJ is specified at the following frequencies – 1MHz, 10MHz and (1/30 UI).

AWG7000 Series
Arbitrary Waveform Generator



DPO/DSA/MSO 70000 Series
Digital Oscilloscope

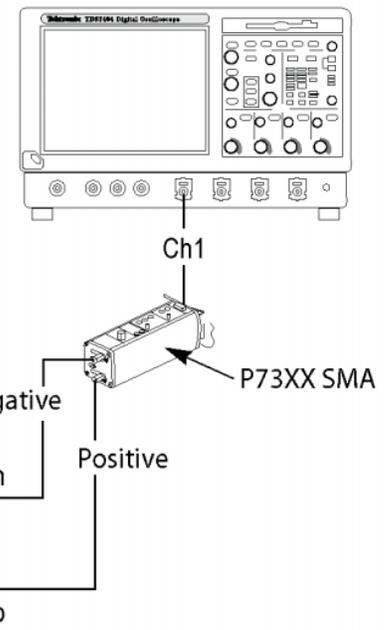


Figure 6-1.

6 Receiver Test Solutions

6.1 Automated M-PHYRX

The M-PHYRX automated software from Tektronix provides following features and benefits for M-PHY receiver testing.

- Simple setup using a tektronix oscilloscope and arbitrary waveform generator for a complete receiver as well as transmitter testing of M-PHY traffic. No other instrument is needed
- Automated testing reduces the complexity of executing receiver tests and enables you to test devices faster
- Integrated ber leverages bit error rate or error count testing using oscilloscope-integrated ERRDT software in the background for all
- Gears (a and b). No external/extra hardware is required to perform BER testing
- Modify the test setup according to the DUT/device configurations such as the high-speed gear, test time or loopback duration, etc.
- Detailed test reports provide a pass/fail summary table, with additional information such as test setup details, signal types, bit error, execution time, etc. for each measurement

6.1.1 M-PHYRX Loopback Initiation and Retention

Before the Receiver test can start, the device under test must be put in the proper test mode, called Loopback, where the DUT loops the incoming signal at Rx directly to the Tx port. Once the Loopback is set on the DUT, then the Arbitrary Waveform Generator sends a Burst mode signal with recommended patterns for all measurements. The M-PHYRX Automation software will allow the user to configure the Loopback settings initially, and retain them for subsequent test executions by sending the signal continuously during the transition from one test to another

6.1.2 M-PHYRX ease of Testing with Pre-calibrated Patterns

The AWG (Arbitrary Waveform Generator) patterns are generated and factory calibrated to ensure the impairments are within the specification with given golden accessories. This simplifies the number of patterns as well as limits the time-consuming calibration routines. Both the AWG and Oscilloscope Error Detector work together concurrently in Loopback mode, and pre-calibrated signals enable you to perform each measurement within three minutes of time.

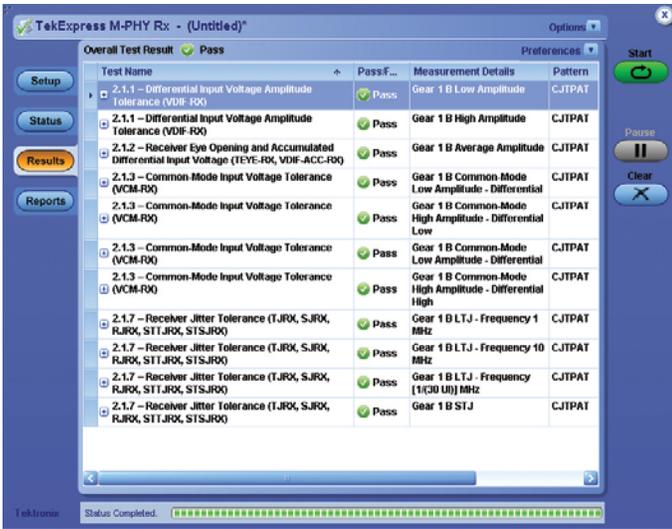


Figure 6-2.

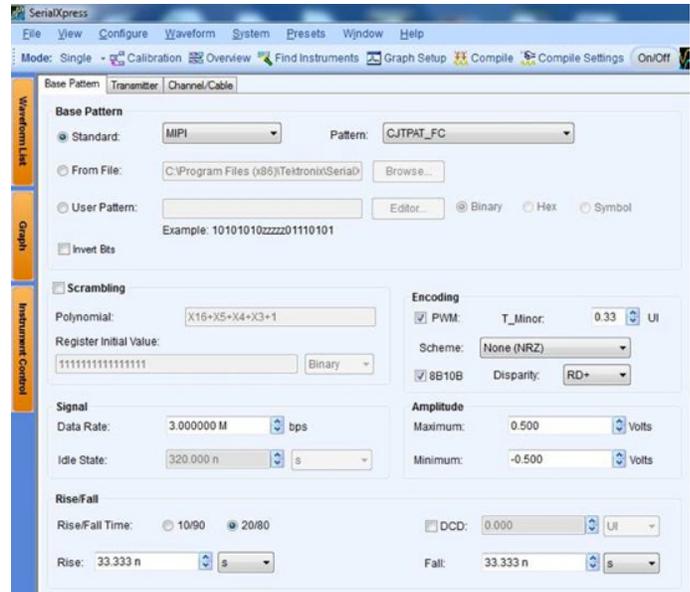


Figure 6-3.

6.1.3 Simple 2-box Test Setup, and Easy Test Execution

Test setup and test execution is very simple with the M-PHYRX automation software. The test setup connections are very minimal, as it involves only two pieces of equipment for M-PHYRX. M-PHYRX controls the Arbitrary Waveform Generator (AWG) and Oscilloscope Error Detector. The TekExpress software provides a Graphical User Interface (GUI) and an intuitive workflow through setup and testing.

6.1.4 Results and Reports

Detailed Test Reports provide a Pass/Fail Summary Table, with Additional Information such as Test Setup Details, Signal Types, Bit Error, Execution Time, etc. for Each Measurement.

6.2 Additional Receiver Test Tools

6.2.1 Test Setup with Arbitrary Waveform Generator

- Supports Flexible Signal Impairments using Serial Express Optionally for Characterization
- Supports Jitter Insertion and Pulse Width Modulation (PWM) according to the Base Specification v1.0
- Supports Testing the DUT in both Loopback and Non-loopback Mode

6.2.2 SerialXpress for Customized M-PHY Patterns Generation

SerialXpress - 'Advance Jitter Generation tool' is an application which runs on AWG (Arbitrary Waveform Generator). This is a generic tool for used for many High speed serial standards, which also caters for all the waveform generation needs of M-PHY. Just to mention a few SerialXpress supports NRZ and PWM signaling types. Jitter or impairments like Rj, SSC, Channel emulation, de-emphasis etc. Given in Figure 6-3 is a screen shot of the Application.

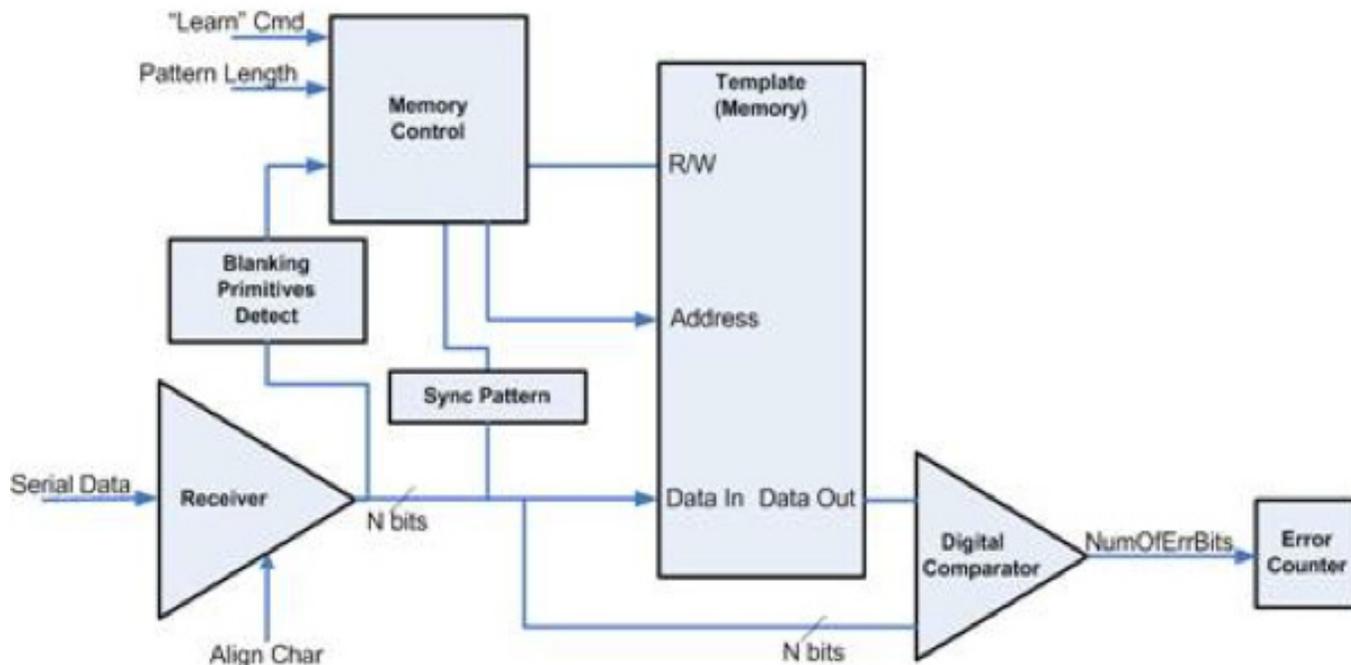


Figure 6-4.

6.2.3 Oscilloscope Error Detector

In M-PHY transmitter, 8b/10b is a line code used to achieve DC-balance and bounded disparity. As the scheme name suggests, 8 bit of data are transmitted as a 10-bit entity called a symbol, or character. The low 5 bits of data are encoded into a 6-bit group (the 5b/6b portion) and the top 3 bits are encoded into a 4-bit group (the 3b/4b portion). These code groups are concatenated together to form the 10-bit symbol that is transmitted on the wire. The data symbols are often referred to as D.x.y where x ranges from 0–31 and y from 0–7.

In M-PHY receiver test solution, error detection is done using oscilloscope based bit error detector. This bit error detector requires two input parameters, first one being the bit sequence (SOF) which it uses for synchronization and second one is the bit length. Bit length specifies the number of bits which need to be stored in memory and later used for comparison and error detection. Synchronization pattern does not have to be at the beginning of the signal test pattern, just somewhere in the signal test pattern, as the fixed length signal test pattern is sent repeatedly by signal generator.

Principle of operation of Oscilloscope Error-Detector

The following conceptual Bit Error Detector Block Diagram shows that given the signal test pattern Length, a Sync Pattern, an Align Character, and a PI “LEARN” command, the Error Detector can acquire the test pattern and store it into the hardware Template Memory. It shows that once the Template Memory is written the Digital Comparator can compare the signal to the Template in order to detect errors and increment the Error Counter. It shows that Align Primitives or Skip Order Sets can be detected and ignored/rejected if desired. It shows that Align Character must be known in order to keep the Receiver aligned to 10-bit character boundaries.

The align character is a 10-bit character with both RD+ and RD- disparity values and must actually be present in the signal test pattern in order to keep the receiver aligned to 10-bit character boundaries. The sync pattern is a unique 10-, 20-, 30-, or 40-bit sequence (one to four 10-bit characters) that must actually be present in the signal test pattern in order to align the signal to the hardware Template Memory so that bit-by-bit comparisons can be made. The sync pattern does not have to be “at the beginning” of the signal test pattern, just somewhere in the signal test pattern, as the fixed-length signal test pattern is sent respectively by the signal generator. Thus, the Bit Error Detector requires you to have some knowledge of the signal test pattern contents.

8b10b Coding and Script Configurations

8b10b is a line code which maps 8-bit symbols to 10-bit symbols. 8b10b encoding is used to achieve DC balance and provide enough state changes to allow reasonable clock recovery. 8b/10b encoded data will not have more than five 1s or 0s in a row. This helps to reduce the demand for lower bandwidth limit of the channel necessary to transfer the signal. In 8b10b encoding, each data byte has two different symbols, one selected to have slightly more “1” values and the other to have slightly more “0” values. These different symbols are called positive and negative disparity, and the transmitter keeps track of the disparity and selects the appropriate symbol for the next byte to compensate for any disparity introduced by the previous symbol.

In M-PHY, all information communicated inside burst state shall be 8b10b encoded. Coding of each byte consists of a 5b6b and a 3b4b sub-block encoding.

At M-PHY high speed data rates, Tektronix oscilloscope error detector supports bit error detection. Bit error detector requires following inputs

- Source – the channel on the oscilloscope to which the signal is fed as input
- Data rate – data rate of the signal
- Synchronization symbol – It is a unique sequence (10, 20 or 30 bits) that will occur in the data pattern
- Test pattern length – length of the bit pattern (number of bits) that occur between two synchronization symbols

Scope error detector can be invoked using following programmatic interface (PI) commands

- ***RST** – This will reset the oscilloscope
- **TRIG:A:TYPE SERIAL** – Selecting trigger type as serial
- **TRIG:A:SERIAL:SOURCE Ch1** – Selecting Ch1 as the source for trigger (data is fed to channel1 of the oscilloscope)
- **TRIG:A:SERIAL:CODE s8b10b**
- **TRIG:A:SERIAL:STANDARD custom**
- **TRIG:A:SERIAL:BITRATE 1.248e9** – specifying the data rate of the signal

- **TRIG:A:SERIAL:ERRORDETECTOR:PATTERNNA ME “Name to be displayed on screen”** – Name that gets displayed on screen. This is used to provide a visual feedback to the user that the recalled setup file is appropriate for the signal being tested. It has no function in driving oscilloscope hardware or software.
- **TRIG:A:SERIAL:ERRORDETECTOR:TYPE BIT** – specifying the type of error detector
- **TRIG:A:SERIAL:ERRORDETECTOR:STANDARD ANY8B10B**
- **TRIG:A:SERIAL:ERRORDETECTOR:BIT:LENGTH <Num>** – specifying the length of the bit pattern that occur between two synchronization symbols.
- **TRIG:A:SERIAL:ERRORDETECTOR:BIT:SYNCPATTERN “0011111010”** – unique synchronization pattern
- **TRIG:A:SERIAL:ERRORDETECTOR:STOPWHEN <MANUAL | COUNT | TIME | ERROR>** –
 - MANUAL is the default, so Stop Test Action is used to stop the test.
 - COUNT stops the test when DURATION:COUNT comparisons have been made. The comparisons may be Bit, Frame, Symbol, or Character as appropriate for the TEST:TYPE.
 - TIME stops the test when DURATION:TIME elapses. Technically, DURATION:TIME is converted to Bits, Frames, Symbols, or Characters as appropriate for the TEST:TYPE and that value is used as the stopping condition.
 - ERROR stops the test when number of errors >= ERRORLIMIT.
- **TRIG:A:SERIAL:ERRORDETECTOR:DURATION:COUNT <Num1>** – defines test duration count as number of bits to be tested. A value of -1 means “count forever” and is the default
- **TRIG:A:SERIAL:ERRORdetector:ERRORLIMIT <NR1>** - defines the error limit. When this limit is reached the error detector will exit. When STOP and there is ERROR, the test stops when the number of errors is greater than or equal to the ERRORLIMIT. When STOP and there is no ERROR, ERRORLIMIT does not apply.

Apart from supporting bit error detection for 8b10b encoded data, oscilloscope error detector also supports bit error detection for NRZ data (PRBS9) at 312 Mbps.

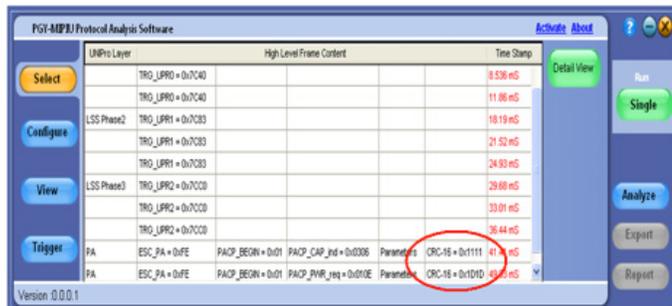


Figure 6-2. PGY-UPRO with CRC counters decoded from an M-PHY UniPro packet.

6.2.4 Non-loopback mode Receiver Testing

Following are the steps to perform RX tests in non-loopback mode

- Send the Known signal at the RX input compatible to protocol content (UniPro or LLI) on single lane with impairments (Amplitude or Jitter, etc one impairment parameter at time according to specification).
- DUT receives these signal internal decode it and check it for CRC, perform the Error check and If RX unable to tolerate, detects error, then Internal Error counter gets incremented.
- The Error counter content needs to be read for RX test , There are Two options, one option is customer can read the Error counter content. The second option is We can send the Query pattern (complied to MPHY and type of Protocol) at the RX input, The response will be available at TX output which we can acquire it suing oscilloscope and Decode it to get the Error counter content. So, Using a Protocol decode software (example PGY-UPRO or PGY-LLI), we can read the data content and arrive at Errors.

7 M-PHY Protocol Testing

7.1 UniPro/ LLI/ DigRFv4 Protocol Decode Analysis

Design and Test engineers working on M-PHY hardware/ firmware designs for UniPro/ LLI/ DigRFv4 applications need to monitor and debug UniPro/ LLI/ DigRFv4 protocol interfaces respectively to ensure reliable operation of the M-PHY system. High Speed Serial design/test engineers prefer easy-to-use instruments such as oscilloscopes for electrical and protocol testing in a single instrument. The oscilloscopes normally provide extensive details about electrical characteristics of the signal. But engineers need more information such as packet contents at different protocol layers. Manually interpreting the protocol layer information using oscilloscope data is time consuming and prone to human errors in a versatile M-PHY protocol applications.

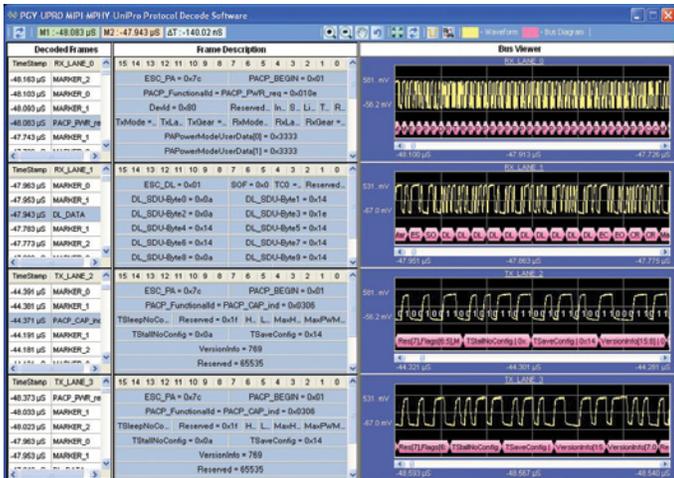


Figure 8-1.

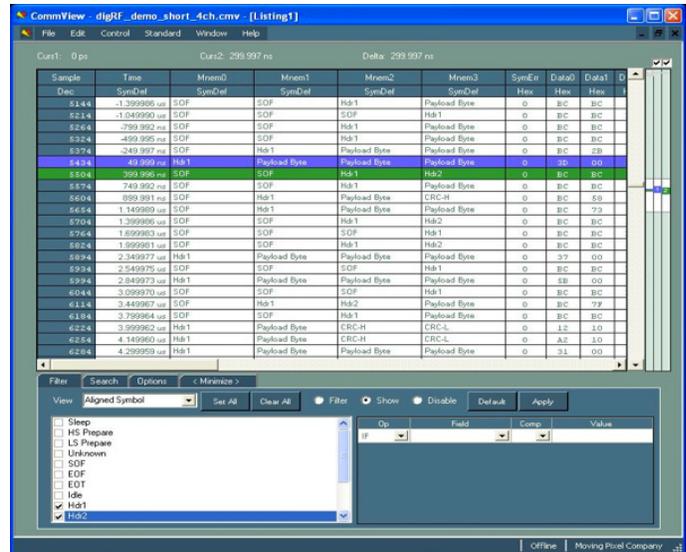


Figure 8-2.

8 Protocol Test Solutions

The PGY-UPRO/ PGY-LLI Protocol Decode Software offers extensive protocol decoding for M-PHY UniPro and LLI protocol standards. Using this software, design and test engineers can automatically make accurate and reliable decoding of multi-lane M-PHY UniProg/LLI traffic acquired by Tektronix, DPO/DSA/MSO7000 oscilloscope series. Trigger configuration of PGY-UPRO/ PGY-LLI leverages the Oscilloscope option ST6G serial trigger features and helps to trigger the UniPro and LLI specific events. The software supports automated CRC computation to monitor CRC errors in the UniPro/ LLI protocol packet.

The MPHVIEW Protocol Decode Software automatically recognizes M-PHY data speeds, disassembles, and displays the M-PHY decoded data in different readable-data formats of DigRFv4 protocol. The software acquires up to 4 lanes of M-PHY DigRFv4 data traffic at a time, and supports filter and search on the decoded traffic.

9 Conclusion

Design and Test engineers working on MIPI M-PHY technology are facing several challenges. Testing M-PHY transmitter interfaces require approximately 1000 testcases in different combinations of Gears, sub-Gears, Amplitudes, and Termination for each lane under test. Testing M-PHY Receiver interfaces require generating different mix of patterns such as NRZ and PWM, with impairments such as ISI, DC-common mode, Jitter components, etc. In addition, Receiver testing also requires testing for Bit-Error-Rates and error-counting in loopback and non-loopback approaches.

Automated test tools such as Tektronix M-PHYTX and M-PHYRX solutions will provide single-button test setups for comprehensive test case coverage for testing both transmitter and Receiver interfaces of M-PHY designs. Further, State of the art tools like SerialXpress and DPOJET analysis enable generating customized patterns, performing additional characterization and debug/failure analysis.

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Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit www.tektronix.com



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