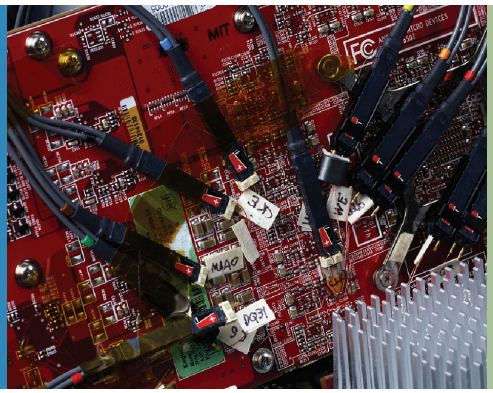

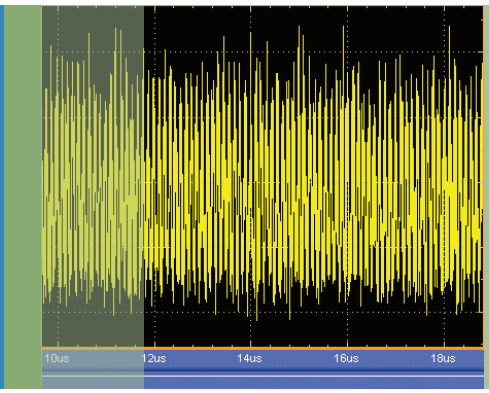

Debug and Validation of High Performance Mixed Signal Designs

Application Note

Introduction

Modern embedded and computing systems have become progressively more powerful by incorporating high-speed buses, industry standard subsystems, and more integrated functionality in chips. They have also become more complex, more sensitive to signal quality, and more time consuming to troubleshoot.

While standards exist for many technologies commonly used within high performance digital systems, a major test requirement is to ensure that all elements are synchronized and perform as a seamless, integrated whole. End devices may contain multiple subsystems, some of which need to communicate with one another and with the outside world. This is an extension of integration testing where the timing of integrated functions and communication between subsystems must be verified. This testing requires tools that enable evaluation of not only a single element but also an entire system.

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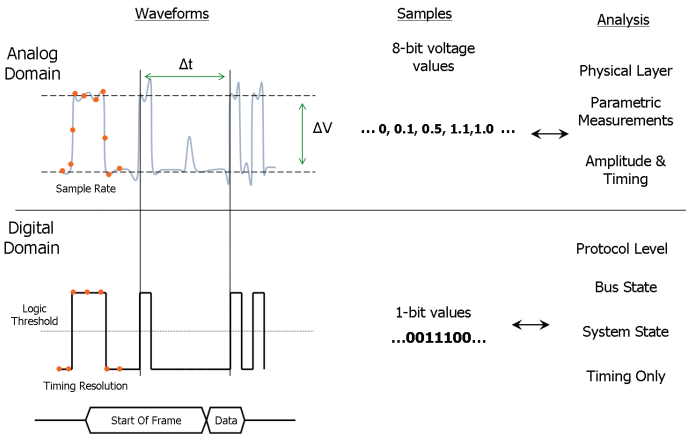

Figure 1. Analog and digital measurement differences.

Figure 2. MSO70000 Series can provide time correlated views of analog and digital signals.

System testing overview

In step with increasing functionality and performance, engineers often have to work with both analog and digital signals in their designs. This complicates the job of testing, requiring specialized tools to see what is happening at various test points on the device under test. Analog testing, for example, requires precise voltage values for performing physical layer analysis such as amplitude, timing or eye diagram measurements. The oscilloscope has been the primary tool for this job. Digital system test uses only logic state values and may use timing information only. By time correlating many digital signals bus or protocol level analysis can be performed. Digital system test and debug may require triggering on specific bus cycles such as a memory read or write. Logic analyzers with wide bus capabilities are typically used for digital system test.

In many cases, when hardware and software engineers are working together to troubleshoot the root cause of a specific problem, they require a view of information on a bus - both its electrical representation and also at a higher level of abstraction like the decoded view of a serial bus protocol. Many designs have a large number of hardware components for executing specific tasks that may be located on different parts of the circuit board. To verify interaction between components, engineers need to have a system-level view of the DUT. The challenge is to make sure that the component operations are synchronized, which means that the test equipment needs to be able to provide accurate information on timing performance in addition to viewing and analyzing data at higher levels of abstraction and analysis.

A mixed-signal oscilloscope (MSO) provides analog signal characterization with digital bus event and timing analysis for the ideal system debugging tool. Mixed analog and digital design and validation benefits from three key MSO capabilities: timing correlation, state visibility, and data qualification.

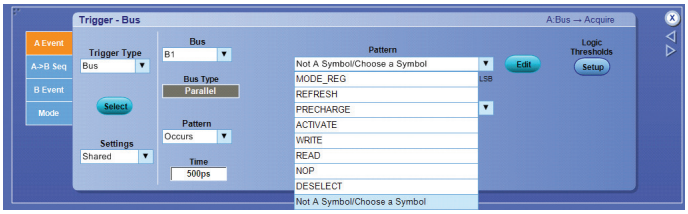

Figure 3. Triggering with user-definable Bus definitions.

Figure 4. Bus qualified trigger of memory read cycle.

Analog and Digital Correlation

Time-correlated analog and digital signal information can lead to more efficient verification and debugging. In mixed-signal control systems, software-based control loop behavior can be correlated with analog stimulus and response signals. In system debugging, incorrect digital states (e.g. invalid character) can be more easily traced to low-level signal effects (e.g. data dependent jitter) in the physical layer.

Understanding the context in which an event occurred can be valuable while debugging digital systems. For example, what memory location was being accessed? Where did this packet of information originate? What was the state of the ASIC when that bus fault occurred? Low-level or physical layer details are often needed to identify root cause but often the most efficient way to trace issues is to understand in what state was the larger system. Being able to capture several views of signaling as it flows through a system can more quickly lead to critical insight.

Often it is necessary to analyze specific cycle types, such as signal integrity during read cycles or write timing jitter for a specific bank of memory. Sophisticated signaling schemes such as in DDR can complicate debugging. When cycle information is distributed across several digital signals it takes sophisticated triggering to respond to it in real time. Thus, effective debugging may include detecting signal faults only during specific bus cycles. Digital pattern qualification can be applied to logic-fault trigger types to detect signal faults in real time, such as a glitch during a Read.

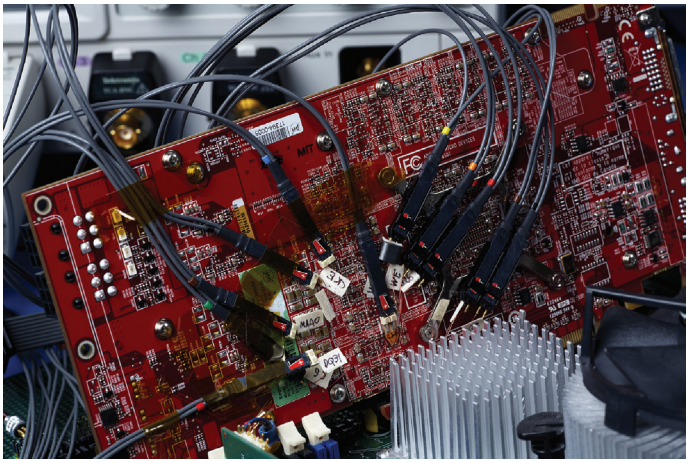

Figure 5. P6780 differential logic probes connected to GDDR5 video graphics card.

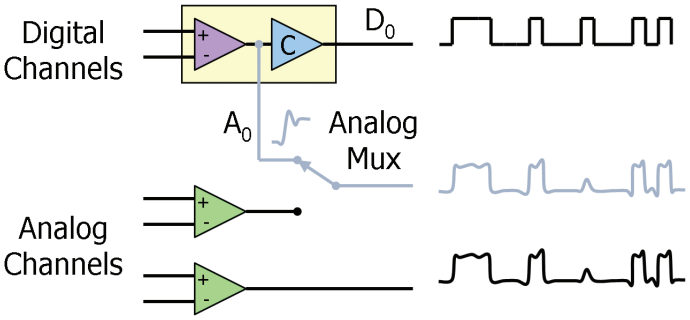

Figure 6a. Block diagram of Analog Mux.

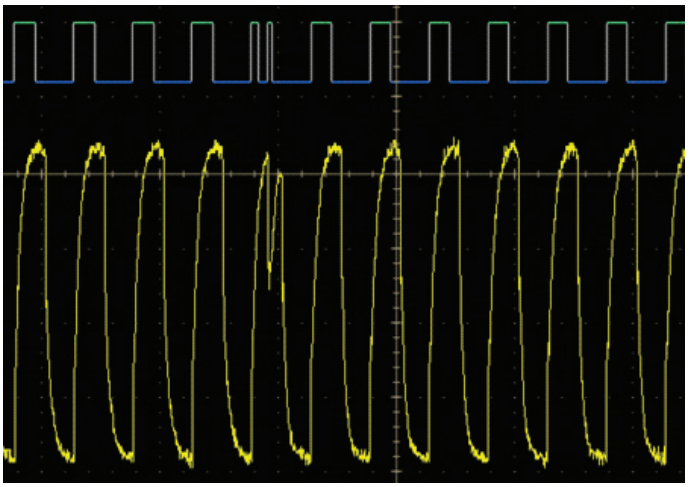

Figure 6b. Glitch shown in digital and analog view using iCapture. Both the digital and analog signals were acquired from a single probe.

Signal Access

Attaching a probe to a device poses another challenge. The small physical size of the devices, the large number of points on the board that need to be probed, and the fact that any probe adds capacitive loading altering the operational characteristics of the device are all factors that add to probing challenges. Probing solutions need to be designed to minimize the capacitive loading, make it easier for the engineer to connect to the device, and also be able to quickly ascertain which probe (or probe lead) is correlated to which trace on the screen of a test instrument.

The MSO70000 series Mixed Signal Oscilloscopes provide high performance, 16 channel logic probes like the P6780 Differential Logic Probe. The P6780 can connect to small vias and components using accessories designed for solder-in connections.

Analog Mux

The MSO70000 series includes the iCapture™ analog mux feature that allows engineers to view a signal connected to any of the 16 logic probe connections in simultaneous analog and digital views. There are two key benefits of the iCapture capability. First double probing is not required to view signals in both digital and analog domain. This helps ensure optimum signal fidelity of the device under test by reducing the capacitive loading introduced by the test equipment. The second benefit is improved timing and precision that is available across any of the 16 digital channels. The user can turn on the analog signal through the oscilloscope's user interface or develop software routines to turn on or off the analog mux in an automated fashion.

Mixed Analog and Digital Devices

Mixed signal design problems are difficult to debug and often require advanced measurement techniques across multiple domains. The MSO70000 provides both the analog and digital signal analysis capability to examine the interaction of the hardware and software in a target system. The following are three examples of using the MSO70000 to debug mixed analog and digital systems including high speed serial technologies, FPGA designs, and RF subsystems.

High Speed Serial Designs

High speed serial bus architectures, including PCI-Express, HDMI and SATA, provide significant data throughput with additional benefits such as differential signaling, lower pin count and less space for board layout. What all these latest standards have in common are faster edge rates and narrower data pulses, which combine to create unique, exacting demands on designers. As multi-gigabit data rates become common in digital systems, signal integrity - the quality of the signal necessary for proper operation of an integrated circuit - is becoming a paramount concern for designers. One bad bit in the data stream can have a dramatic impact on the outcome of an instruction or transaction.

High performance video systems can incorporate a wide variety of technologies such as RF receivers, video processors, memory and high speed serial interfaces. Figure 7 shows a typical block diagram of a high end set top box. This system has implemented an HDMI interface which operates at 3.4 Gb/s across each of the three data lanes. Figure 8 shows the architecture of the HDMI link including high speed clock and data lines along with the Display Data Channel (DDC) which uses I^2C signaling in standard mode (10 MHz). The DDC line is used for information exchange between the Source (Transmitter) and Sink (Receiver) devices.

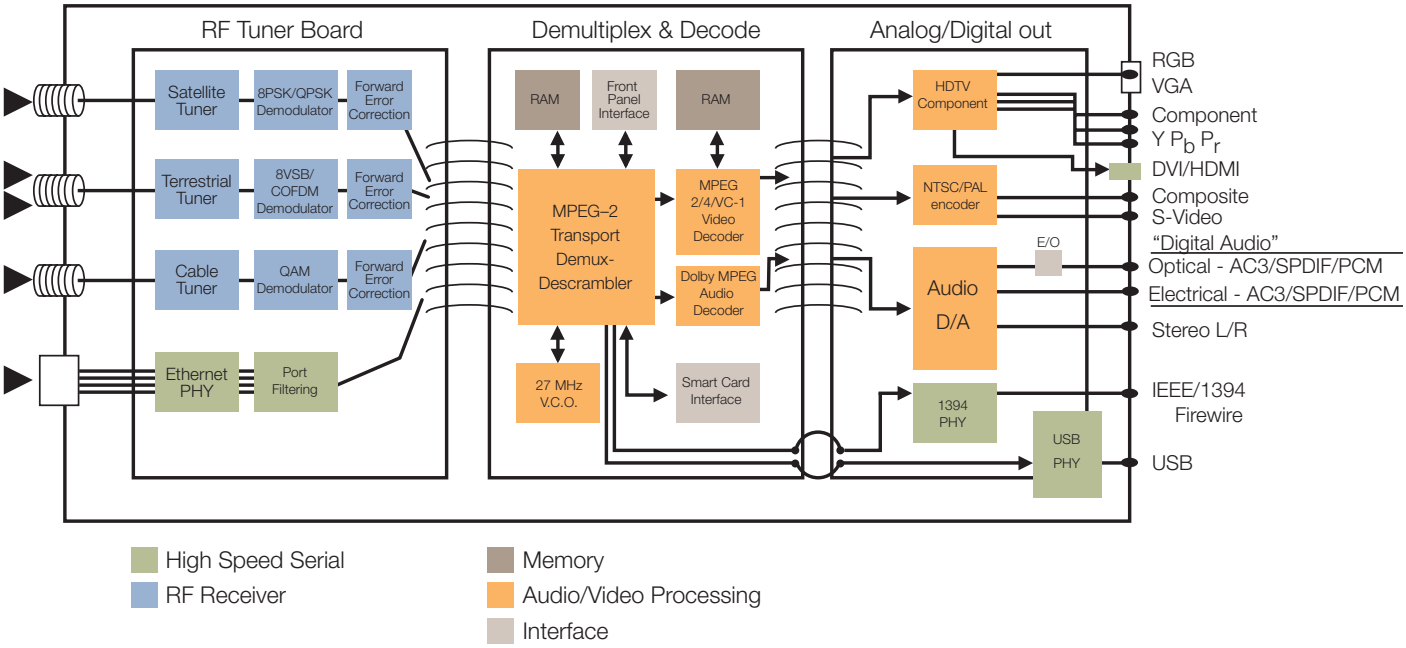

Figure 7. A block diagram of a typical HD Set Top Box.

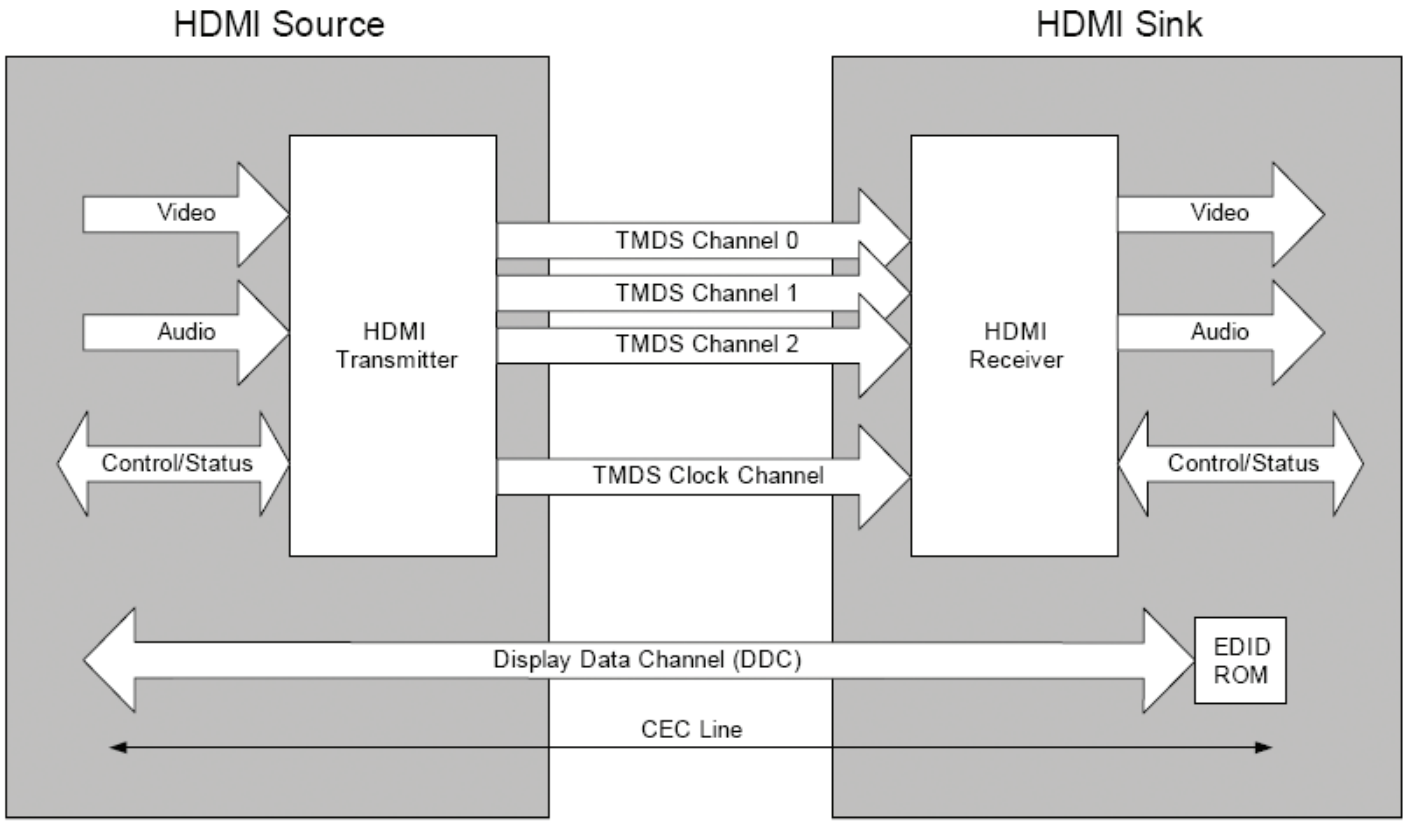

Figure 8. HDMI system architecture.

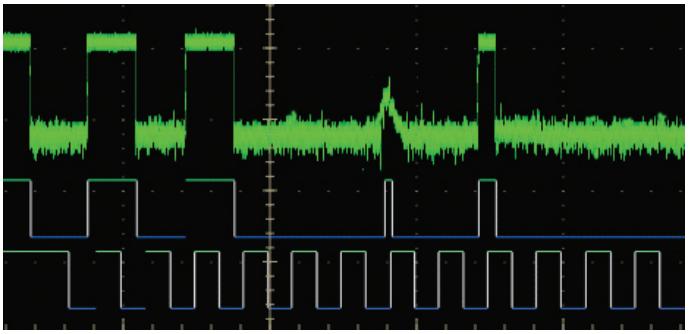

Figure 9. Glitch on I²C SDATA line.

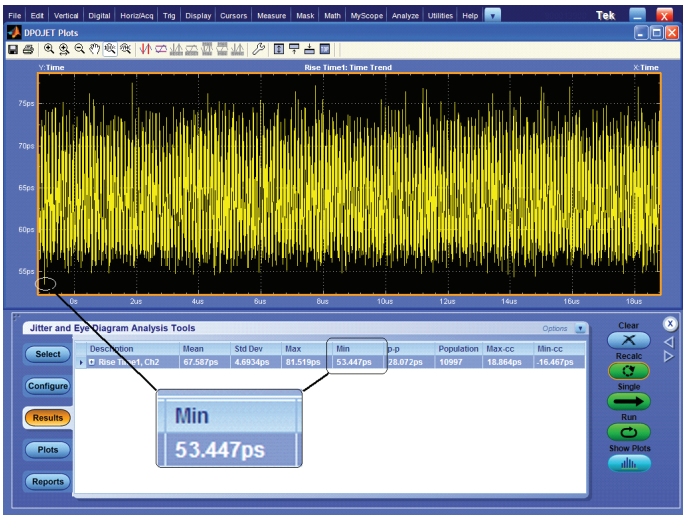

Figure 10. Trend plot of rise times within a 19 us window near the I²C glitch. The fastest edge rate measured is about 53 ps.

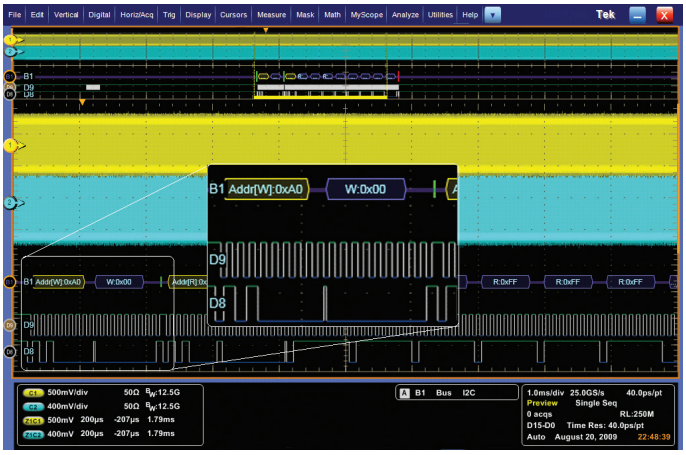

Figure 11. MSO70000 decodes address 0xA0 after crosstalk issue is resolved.

This design required debug as the output to the monitor would turn off intermittently. First the physical layer was checked for functional operation and each lane passed eye diagram and jitter measurements. After the high speed clock and data lines were measured, the I²C control lines were monitored for error codes or invalid data. In normal operation the DDC uses addresses 0xA0 and 0xA1. However after the MSO70000 captured and decoded the I²C traffic an incorrect address would sometimes be asserted during power up. Figure 9 shows the SDATA line in digital and analog format using the iCapture tool on the MSO70000. Based on the analog signal view it appeared there were crosstalk or other noise coupling effects that corrupted the I²C traffic.

In order to find the root cause of the glitch adjacent lanes were analyzed and edge rates were evaluated across each high speed lane. Figure 10 shows a 19 us time window with a trend plot of edges occurring close to the glitch. This analysis provides some insight into what caused the signal anomaly. The minimum measured rise time of 53 ps was much faster than the 90 to 100 ps edge rates typically found in HDMI systems. The design was then modified to slow the edge rates and the data and clock shielding lines were also improved. Figure 11 shows the correct I²C transactions, including addresses 0xA0 and 0xA1 and the acknowledgement bit before the Write data.

Field Programmable Gate Arrays (FPGA)

The phenomenal growth in design size and complexity continues to make the process of design verification a critical bottleneck for systems based on Field Programmable Gate Arrays (FPGAs). Limited access to internal signals, advanced FPGA packages, and printed circuit board (PCB) electrical noise are all contributing factors in making design debug and verification the most difficult process of the design cycle.

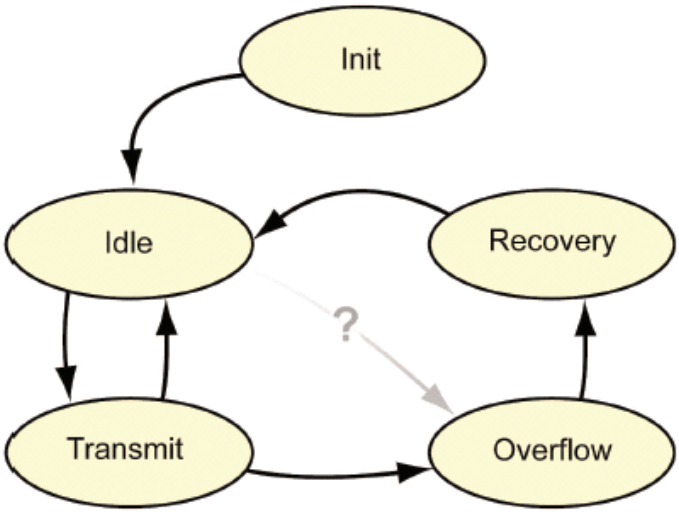

Figure 12. Debug Port state machine of the PCI Express receiver.

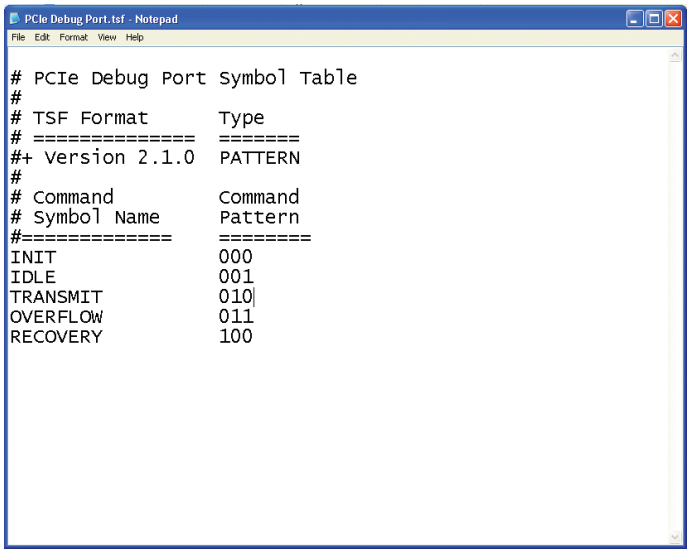

Figure 13. Tektronix symbol file for PCIe Debug Port.

When faults occur in FPGA based designs, engineers can use the MSO70000 to see analog events such as the input and output signals and power supply lines in addition to the digital lines that show them internal status of the FPGA logic. Potential problems that can be debugged include:

- Situations that were not accounted for in simulation, e.g. a power supply problem
- Cross-talk between high speed lines caused by a stronger line driver affecting an adjacent line that only occur when a set of drivers turn on together
- Incorrect SW commands sent to an state machine resulting in unexpected behavior
- State machine logic errors, unlocked phase lock loops, and FIFO overruns

Let's see how the MSO70000 was able to debug an FPGA used as a bridge between a PCI Express link and DDR memory bus. This example shows how monitoring FPGA states externally can speed debug of state machine problems in FPGAs.

PCI Express transmitter/receiver pairs often include not only a serial link, but also a built-in “debug port.” This parallel output delivers real-time data summarizing the transactions occurring within the device. With debug ports on both the transmitter and the receiver, developers can monitor the health of the transmission link and localize many types of problems to either the transmit or the receive side. Figure 12 represents a state machine that might be found within a PCI Express serial receiver. The simplified interactions shown here symbolize a routine link procedure, with the black arrows indicating legal state transitions. Figure 13 is a screen image showing an example Tektronix symbol file (.tsf) created in Notepad to enable analysis of the Debug Port on the MSO70000. Figure 14 shows an acquisition taken from a PCI Express serial link. An error on the bus has caused the MSO to trigger on bus violation. Because of the good signal quality we can visually tell the problem does not stem from an underlying analog problem. The finding in Figure 14 strongly implies a logic issue caused by a timing problem or other digital conflicts.

Because the serial data errors coincide with the Overflow state on the debug port, and because the serial data is driven by the SERDES it is reasonable to assume that the problem is timing-related and originates within the SERDES. At this point there may be several potential troubleshooting strategies, influenced by architectural considerations or other debug findings.

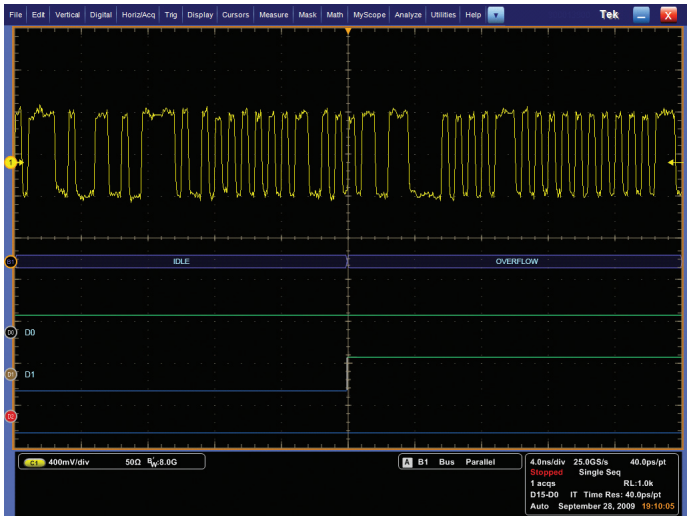

Figure 14. The bus error (OVERFLOW state) coincides with an incorrect state change in the Debug Port state machine. This implies a timing problem within the SERDES, which may stem from errors in the FPGA synthesis process.

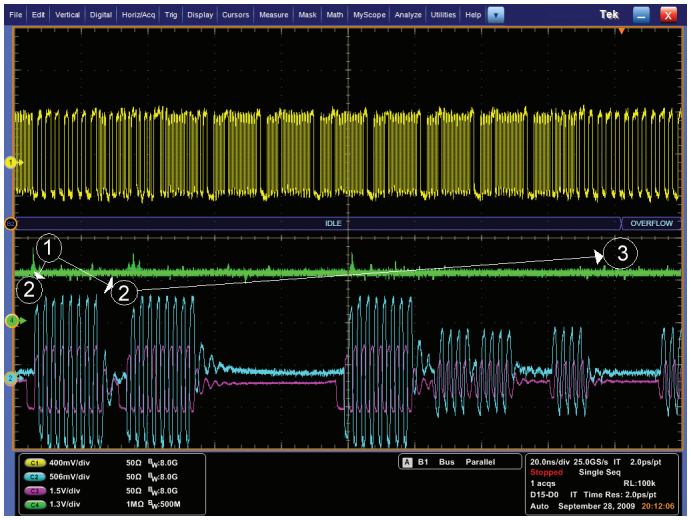

Figure 15. Ground bounce (1) causes setup and hold violations on Read data (2) which returns invalid data to PCIe bus.

In an FPGA the design is transformed into functional elements defined by the programmer. This "transformation" process is known as synthesis, since it literally synthesizes the desired functions using its internal gates. Knowing this, the astute designer will troubleshoot the error first by double-checking the FPGA synthesis results to make sure the timing of all state machine transitions is correctly implemented.

If that doesn't reveal the problem's source, a second pragmatic step is to route other signals to the debug connector to trace the device's behavior. For example, after evaluating the Current State data as shown in Figure 12 the FPGA might be reprogrammed to deliver the "Next State" data to the debug port. This could reveal issues that are not seen in the Current State, and of course there are even more states that can be investigated beyond that.

Another common approach to debugging FPGA designs is to follow the data flow backwards from the error source to determine root cause. After further investigation the MSO70000 was able to show that a power supply lin was inducing noise on the DDR memory bus. Right before the FPGA state machine put the PCIe link into an Idle state a memory Read request was issued. Switching noise caused issues with the memory bus which in turn propagated back into the PCIe bus. This was the primary cause of the FPGA state machine error.

Frequently, tracing a system problem involves much more than just following a glitch back to its source in some logic element. An error on one bus may have its origins—and its impacts—on multiple buses in the system. For this reason, complete cross-bus analysis has become an indispensable troubleshooting methodology. With the MSO70000 Series, time-correlated digital and analog events are brought into view on a common screen, thus providing a powerful new tool in troubleshooting FPGAs and multi-bus systems. Cross-bus analysis makes it possible to see simultaneous interactions throughout the system, speeding efforts to track down not just errors, but also their root causes.

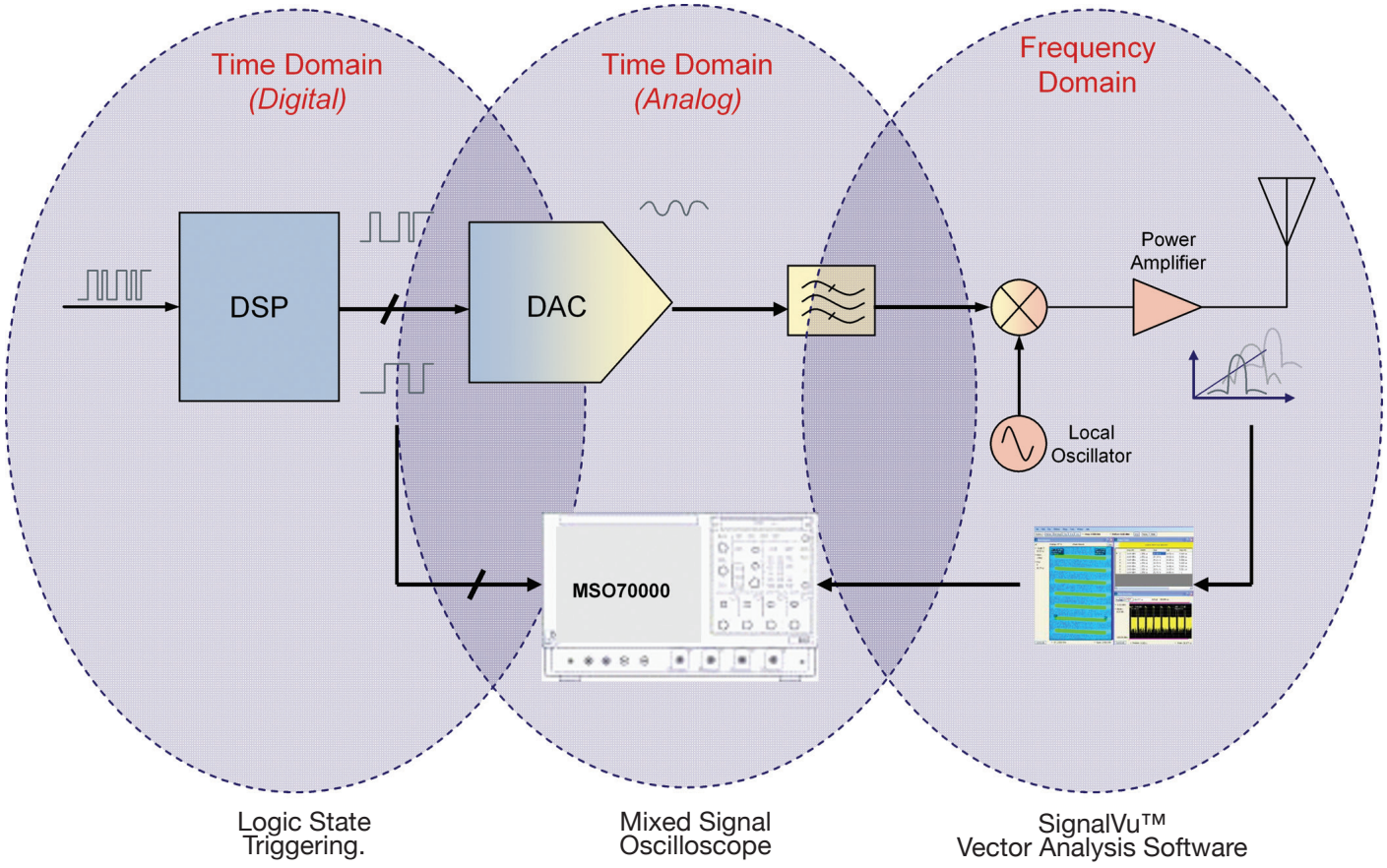

Figure 16. Block diagram of a transmitter and connectivity to a Mixed Signal Oscilloscope.

RF Test

One of the challenges in the design of software defined radios is troubleshooting and mitigation of hardware and software errors. As DSP controls more and more of the analog functionality, illegal state or filter values in the digital baseband portion of a design can manifest themselves as RF spectrum errors when they are propagated to the filtering and amplifier portions of a transmitter.

Figure 16 shows the connectivity of the MSO for complex multi-domain analysis. Not only can the digital and analog domains be analyzed, but with the inclusion of vector signal analysis software, a thorough analysis that includes the frequency domain can be performed on the same data acquisition.

For this example, the MSO logic trigger is set to catch an illegal state value to the input of the Digital-to-Analog Converter (DAC). The logic trigger for an all “1” state value (0x3F) triggers the acquisition. The correlated view of the analog signal in Figure 17 is shown delayed in time, about 34 ns. This represents the absolute delay in the DAC conversion process of this high-speed device.

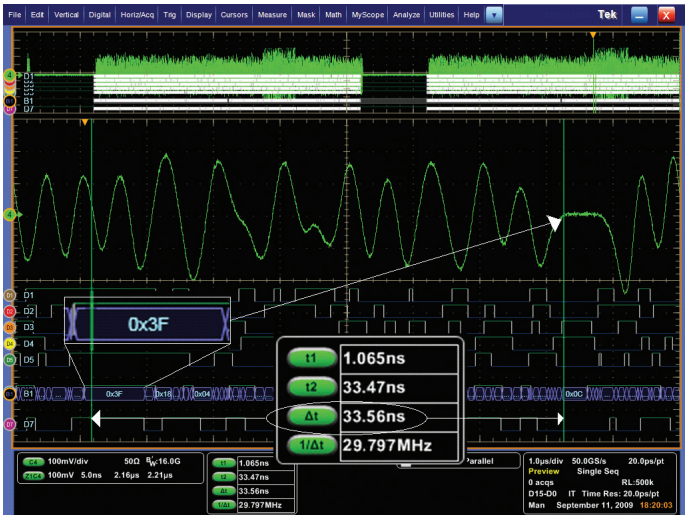

Figure 17. The integrated view of the logic states at the DAC and Analog output.

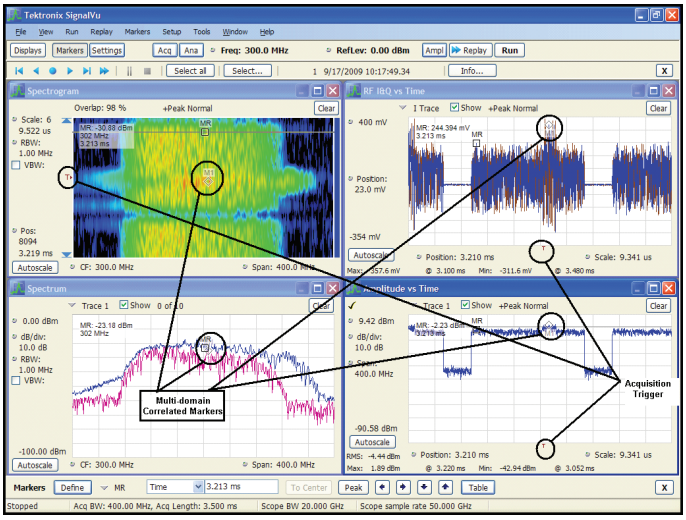

Figure 18. SignalVu enables time correlated multi-domain views for in-depth analysis.

This analysis enables the correlation of the logic state to the wide pulse appearing on the MSO's analog channel. The time domain view of the RF signal may not give us the complete view of the impact this might have on our software radio design, so further correlated analysis of the RF performance is required.

To assess the RF performance of the signal on the same acquisition, SignalVu™ software can be used directly on the same data set. Figure 18 shows RF analysis on the same data set acquired for Figure 17. The logic state trigger has been used to trigger the data set and the SignalVu analysis performs the RF analysis.

In this example, Discrete Fourier Transforms (DFTs) are performed to show the Spectrogram and Spectrum frequency domain analysis, and time sampled data is displayed as RF I&Q vs Time and Amplitude vs Time.

Time correlated markers have been turned on to demonstrate the time-correlation of the RF analysis for different views. It can clearly be seen that the illegal state values triggered at the DAC resulted in a spectral regrowth at RF. The RF regrowth can be traced back to the digital state in the block diagram, thus ruling out a hardware problem in the analog portion of the transmitter.

Summary

Digital designers need to quickly find and analyze a wide range of problems from signal integrity issues such as cross-talk or jitter to bus faults such as setup and hold violations or dropped packets. The MSO70000 Series with 80 ps timing resolution can make precise timing measurements on as many as 20 channels simultaneously. With iCapture, you can quickly view analog characteristics of a digital channel without adding another probe, saving time and minimizing load on the device under test. By triggering and decoding on a bus, invalid states are quickly detected.

High performance digital systems continue to evolve and become more complex, more sensitive to signal quality, and more time consuming to troubleshoot. An MSO can be the right tool to help efficiently analyze and debug systems and bring products to market even faster.

Contact Tektronix:

ASEAN / Australasia (65) 6356 3900
Austria* 00800 2255 4835
Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777
Belgium* 00800 2255 4835
Brazil +55 (11) 3759 7600
Canada 1 (800) 833-9200
Central East Europe, Ukraine and the Baltics +41 52 675 3777
Central Europe & Greece +41 52 675 3777
Denmark +45 80 88 1401
Finland +41 52 675 3777
France* 00800 2255 4835
Germany* 00800 2255 4835
Hong Kong 400-820-5835
India 000-800-650-1835
Italy* 00800 2255 4835
Japan 81 (3) 6714-3010
Luxembourg +41 52 675 3777
Mexico, Central/South America & Caribbean 52 (55) 56 04 50 90
Middle East, Asia and North Africa +41 52 675 3777
The Netherlands* 00800 2255 4835
Norway 800 16098
People's Republic of China 400-820-5835
Poland +41 52 675 3777
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Taiwan 886 (2) 2722-9622
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*** If the European phone number above is not accessible, please call +41 52 675 3777**

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